REMARKS

Pending Claims:

In this application, claims 15-30 are currently pending. Claims 18, 21, 25, and 28 have not be altered since filing. Claims 15-17, 19-20, 22-24, 26-27, and 29-30 are amended by this Response. Claims 1-14 have been deleted. Claims 31-41 have been added. Entry of these amendments is respectfully requested.

Rejection under 35 U.S.C. §103

The Examiner has rejected claims 1-14 as being unpatentable over Yato (U.S. Patent No. 4,754,456) or Mori (U.S. Patent No. 4,727,541) in view of Obana (U.S. Patent No. 5,136,587). In addition, the Examiner has rejected claims 1-14 under the double patenting doctrine. The applicant has canceled claims 1-14 and withdrawn them from consideration.

The Examiner has also rejected pending claims 15-30 as being unpatentable over Mori (U.S. Patent No. 4,727,541) in view of Obana (U.S. Patent No. 5,136,587) and Schmidt (U.S. Patent No. 5,812,556). These claims include independent claims 15, 22, and 29. The examiner rejected these independent claims by stating that Mori discloses a method for converting a plurality of parallel data streams into a fiber optic transmission by employing pairs of multiplexers. Obana is claimed to represent a "stacked multiplexer switching arrangement for producing serial data." In examining the Obana reference, it is apparent that Obana shows a traditional multiplexer in which a plurality of parallel data streams (IN1...INn) are sequentially placed on a data bus (30) where a parallel to serial converter 40 converts the data streams to a serial, multiplexed output. This is shown in Figure 4, and described in the Obana specification from column 5, line 44 to column 7, line 5. There is no "multiplexer switching arrangement" described in Obana at column 7, lines 20-40. This section describes only the timing signal used by Obana to select between three input signals in the process of multiplexing them together over a single path. The Schmidt reference cited by the Examiner does describe a switch matrix in the context of a channel director capable of switching data received over channel ports, but Schmidt does not describe any multiplexing in this context.

These three references, whether taken alone or in combination, do not teach or suggest the elements in independent claims 15, 22, or 29. These claims are directed toward a multiple interface facility within a channel director that connects multiple channel ports using a switch matrix. More specifically, claim 15 claims a single channel

director with channel ports, a switch matrix, and the multiple interface facility having a multiplexer and a demultiplexer that could handle such inter-switch communication. Claim 22 focuses solely on the multiple interface facility. Claim 29 claims an entire system including a channel director and a fiber optic data link, with a multiplexer module within the director communicating to a demultiplexer module at a second location. In each claim, the multiplexing is accomplished using a multiplexer module and a demultiplexer module to convert between at least four channel ports and a single output or input data stream.

The office action claims that it would be obvious to combine the channel director of Schmidt with Mori because of the substitution of equivalents. The argument assumed that well known switch matrixes are necessary for the functioning of the cited multiplexer references, and that these switch matrixes had same function as the Schmidt channel director. The Applicant respectfully points out that no switch matrix is necessary for the functioning of the multiplexers of the Mori or Obana reference. A switch matrix allows communication to be selectively switched between incoming and outgoing ports based on a destination address found within the communication. In contrast, Obana and Mori both describe basic multiplexer technology in which multiple data paths are multiplexed together over a single serial path, and then demultiplexed back into separate data paths without any switching of data between data paths. There is no switch matrix, and there is no switching of data between different ports or data paths. The citation to Obana (col. 7, lines 20-40) does not show a switch matrix used as part of a multiplexer.

The applicant acknowledges that the prior art teaches both multiplexing and director class switch matrixes that are used with channel data ports. However, the claimed invention is a unique combination of these technologies useful for combining the switching power of two channel directors. This claimed combination is not suggested by the cited prior art, as there is no suggestion as to the benefits or usefulness of multiplexing multiple channel ports together in the manner of the present invention. As explained in the specification and shown in Figure 3, this arrangement allows for communicating between channel directors in a way that does not require a one-to-one physical link per port. Prior art channel directors, such as shown in Figure 1, required a separate physical link for every port used in connecting the channel directors. Since there is no teaching or suggestion of this improvement anywhere in the cited references,

pending claims 15-30 should be considered a non-obvious improvement over the prior art.

Rejection under 35 U.S.C. §112

The Examiner has rejected claims 15-30 as indefinite for containing the trademark ESCON. In response, the Applicant has amended the claims so as to replace references to "ESCON" ports with references to "channel" ports.

New Claims:

Claims 31-41 are new claims relating to multiplexing where multiple parallel input inputs are selectively presented to a parallel to serial converter which also accepts as an input a "binary indicator" (claim 31) or a "time tag" (claim 37 and 40) as part of the input to the parallel to serial conversion. The indicator (or tag) reflects which of the parallel inputs are being presented to the parallel to serial converter, and is useful in demultiplexing without the need for stuffing synchronization bits. These claims are supported by the Specification as originally filed and are not taught in the prior art. More specifically, neither Mori or Obana teach the inclusion of such an indicator in the input to the parallel-to-serial conversion (and hence the embedding of such an indicator directly in the serial data stream).

CONCLUSION

All of the claims remaining in this application should now be seen to be in condition for allowance. The prompt issuance of a notice to that effect is solicited.

Respectfully submitted,
COMPUTER NETWORK
TECHNOLOGY CORPORATION
By its attorneys:

Date: 15 October 2004

Daniel A. Tysver
Registration No. 35,726
Beck & Tysver, P.L.L.C.
2900 Thomas Ave., #100
Minneapolis, MN 55416
Telephone: (612) 915-9634
Fax: (612) 915-9637